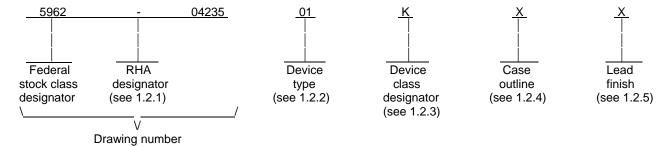
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1. SCOPE

- 1.1 <u>Scope</u>. This drawing documents five product assurance classes as defined in paragraph 1.2.3 and MIL-PRF-38534. A choice of case outlines and lead finishes which are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of radiation hardness assurance levels are reflected in the PIN.
 - 1.2 PIN. The PIN shall be as shown in the following example:



- 1.2.1 <u>Radiation hardness assurance (RHA) designator</u>. RHA marked devices shall meet the MIL-PRF-38534 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.
 - 1.2.2 <u>Device type(s)</u>. The device type(s) identify the circuit function as follows:

Device type	Generic number	<u>Circuit function</u>
01	ACT5028	Resolver-to-Digital converter, Tracking, 16-bit

1.2.3 <u>Device class designator</u>. This device class designator shall be a single letter identifying the product assurance level. All levels are defined by the requirements of MIL-PRF-38534 and require QML Certification as well as qualification (Class H, K, and E) or QML Listing (Class G and D). The product assurance levels are as follows:

Device class	Device performance documentation
K	Highest reliability class available. This level is intended for use in space applications.
Н	Standard military quality class level. This level is intended for use in applications where non-space high reliability devices are required.
G	Reduced testing version of the standard military quality class. This level uses the Class H screening and In-Process Inspections with a possible limited temperature range, manufacturer specified incoming flow, and the manufacturer guarantees (but may not test) periodic and conformance inspections (Group A, B, C and D).
E	Designates devices which are based upon one of the other classes (K, H, or G) with exception(s) taken to the requirements of that class. These exception(s) must be specified in the device acquisition document; therefore the acquisition document should be reviewed to ensure that the exception(s) taken will not adversely affect system performance.
D	Manufacturer specified quality class. Quality level is defined by the manufacturers internal, QML certified flow. This product may have a limited temperature range.

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1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

 Outline letter
 Descriptive designator
 Terminals
 Package style

 X
 See figure 1
 52
 Ceramic, quad flat package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Positive supply voltage range (V _{CC} and V _{DD})	-0.5 V dc to +7.0 V dc
Analog output current (Output shorted to GND)	32 mA
Digital output current (Output shorted to GND)	18.6 mA
Analog input voltage range	$-0.3 \text{ V to } (V_{CC} + .3 \text{ V})$
Digital input voltage range	$-0.3 \text{ V to } (V_{DD} + .3 \text{ V})$
Thermal resistance, junction-to-case (θ_{JC})	1.25°C/W
Maximum junction temperature	135°C
Storage temperature	-65°C to +150°C

1.4 Recommended operating conditions.

Operating voltage range (V _{CC} and V _{DD})	+4.5 V dc to +5.5 V dc
Operating current (I _{CC} + I _{DD})	23 mA
Ambient operating temperature range (T _A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard for Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings. MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http:

^{1/} Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

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2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

- 3.1 <u>Item requirements</u>. The individual item performance requirements for device classes D, E, G, H, and K shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 shall include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. The manufacturer may eliminate, modify or optimize the tests and inspections herein, however the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class. In addition, the modification in the QM plan shall not affect the form, fit, or function of the device for the applicable device class.
- 3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.
 - 3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.
 - 3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.
 - 3.2.3 Block diagram. The block diagram shall be as specified on figure 3.
 - 3.2.4 Functional Block diagram. The functional block diagram shall be as specified on figure 4.
 - 3.2.5 Transfer function diagram. The transfer function diagram shall be as specified on figure 5.
 - 3.2.6 Timing diagram(s). The timing diagram(s) shall be as specified on figure 6.
- 3.3 <u>Electrical performance characteristics</u>. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.
- 3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.
- 3.5 <u>Marking of device(s)</u>. Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked.
- 3.6 <u>Data</u>. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.
- 3.7 <u>Certificate of compliance</u>. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.
- 3.8 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

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	-	TABLE I. Electrical peri	formance charact	eristics.			
Test Symbol		Conditions -55°C ≤ T _A ≤+125				nits	Unit
		$V_{CC} = V_{DD} = +5 \text{ V}$ unless otherwise spec			Min	Max	
DC PARAMETERS	T	T				1	1
Accuracy <u>1</u> /	ACC	Add 1 LSB for total er	ror 1,2,3	01		±5	Minutes
Repeatability			1,2,3	01		1	LSB
Resolution per LSB, (see paragraph 6.8)	RES	10 Bit Mode 12 Bit Mode 14 Bit Mode 16 Bit Mode	1,2,3	01	0.35 0.09 0.022 0.0055		Degrees
		10 Bit Mode 12 Bit Mode 14 Bit Mode 16 Bit Mode			21.1 5.27 1.32 0.33		Minutes
Maximum tracking rate 10 Bit Mode 12 Bit Mode 14 Bit Mode 16 Bit Mode		SC1 SC2 Bits use 0 0 B1 - B1 0 1 B1 - B1 1 0 B1 - B1 1 1 B1 - B1	0 2 4	01	1024 256 64 16		RPS
VCO frequency	f _{VCO}		1,2,3	01	1.05		MHz
ANALOG INPUTS	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	1	1
Voltage between ± analog signal inputs, ±SIN, ±COS, ±REF	$V_{SIN}, V_{COS}, V_{REF}$		1,2,3	01	1.0	1.5	Vrms
Reference input frequency, ±REF	f _{REF}		1,2,3	01	45	30K	Hz
Input impedance	Z _{IN}		1,2,3	01	2.5		ΜΩ
Input capacitance	C _{IN}		1,2,3	01		15	pF
DC voltage bias on -SIN, and -COS	V _B		1,2,3	01	2.0	2.5	Vdc
Input bias current	I _B		1	01	-100	+100	nA
			2		-1000	+1000	
See footnotes at end of tab	ole.						
ST. MICROCIR	SIZE A			596	2-04235		
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	TABLE	I. Electrical performar	nce characteristics	<u>s</u> - Continued.			
Test	Symbol	Conditions $-55^{\circ}C \leq T_{A} \leq +125$	Group subgrou		Limi	ts	Unit
		$V_{CC} = V_{DD} = +5 V_{CC}$ unless otherwise spec	dc	7,1	Min	Max	
DC PARAMETERS - CONT ENABLE, DATA LOAD, INH,							
Input low voltage 2/	V _{IL}		1,2,3	01		0.8	Vdc
Input high voltage 2/	V _{IH}		1,2,3	01	2.0		Vdc
Input leakage current 2/	ILI		1	01	-200	+200	nA
			2		-2000	+2000	nA
Input impedance 2/	Z _{IN}		1,2,3	01	2.5		MΩ
Input capacitance 2/	C _{IN}		1,2,3	01		15	pF
DIGITAL OUTPUTS BUSY, RIPPLE, and CW / CO	CW				_	i	
Output low voltage	V _{OL}	I _{OL} = 1.6 mA	1,2,3	01		0.3	Vdc
Output high voltage	V _{OH}	I _{OH} = -1.6 mA	1,2,3	01	VL _{I/O} 8		Vdc
DIGITAL I/O, B1 - B16 <u>3</u> /	1	1			1	1	
Input low voltage 2/	V _{IL}		1,2,3	01		0.8	Vdc
Input high voltage 2/	V _{IH}		1,2,3	01	2.0		Vdc
Output low voltage	V _{OL}	I _{OL} = 1.6 mA	1,2,3	01		0.3	Vdc
Output high voltage	V _{OH}	I _{OH} = -1.6 mA	1,2,3	01	VL _{I/O} 8		Vdc
Input leakage current 2/	ILI		1	01	-200	+200	nA
			2		-2000	+2000	nA
High-Z leakage current 2/	I _Z		1	01	-200	+200	nA
			2		-2000	+2000	nA
See footnotes at end of tak	ole.						
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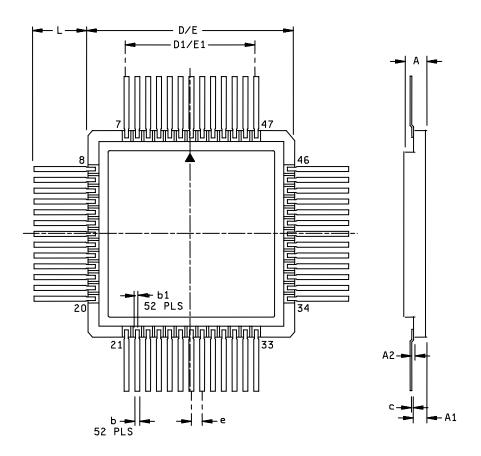
TABLE I. <u>Electrical performance characteristics</u> - Continued.								
Test	Symbol	Conditions	Group A	Device	Limits		Unit	
		$-55^{\circ}C \le T_{A} \le +125^{\circ}C$ $V_{CC} = V_{DD} = +5 \text{ V dc}$ unless otherwise specified	subgroups	type	Min	Max		
AC TIMING, DIGITAL OUTPU	AC TIMING, DIGITAL OUTPUT, $C_L = 50 \text{ pF}$							
BUSY rise and fall time	t _{LH} , t _{HL}	See figure 6	9,10,11	01		85	ns	
CW / CCW, RIPPLE, B1 – B16 rise and fall time	t _{LH} , t _{HL}	See figure 6	9,10,11	01		85	ns	
BUSY pulse width	t _{BPW}	See figure 6	9,10,11	01	300	700	ns	
BUSY to data stable	t _{BDS}	ENABLE = low, See figure 6	9,10,11	01		350	ns	
RIPPLE pulse width	t _{RPW}	See figure 6	9,10,11	01	160	500	ns	
BUSY to RIPPLE	t _{BR}	See figure 6	9,10,11	01		150	ns	
READ DATA, ENABLE and IN	Hare tied to	gether, \overline{DATA} LOAD = log ic Hi,	C _L = 50 pF					
ENABLE low to data stable	t _{ELDS}	See figure 6	9,10,11	01		70	ns	
ENABLE high to data Hi – Z	t _{EHZ}	See figure 6	9,10,11	01		70	ns	
INH low to data stable	t _{ILDS}	See figure 6	9,10,11	01		400	ns	
INH high to data change	t _{IHZ}	See figure 6	9,10,11	01		150	ns	
WRITE DATA, ENABLE and II	NH=logic H	Hi, C _L = 50 pF						
DATA LOAD pulse width	t _{DLPW}	See figure 6	9,10,11	01	200		ns	
Data setup to DATA LOAD	t _{WDS}	See figure 6	9,10,11	01	60		ns	
Data hold	t _{WDH}	See figure 6	9,10,11	01	10		ns	

^{1/} Accuracy applies over the full operating power supply voltage range, Full operating temperature range, reference frequency range, 10 percent signal amplitude varation, and 10 percent reference harmonic distortion.

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^{2/} Parameter shall be tested as part of device characterization and after design and process changes. Thereafter, parameters shall be guaranteed to the limits specified in table I.

^{3/} All unused inputs shall be tied to ground. Bit 1 is always the MSB.



Symbol	Millimeters		Incl	hes
	Min	Max	Min	Max
Α		2.54		.100
A1	1.42	1.78	.056	.070
A2	0.20	REF	.008	REF
b	0.58 TYP		.023 TYP	
b1	0.43	TYP	.017 TYP	
С	0.13	0.20	.005	.008
D/E		24.28	.956	
D1/E1	15.11	15.37	.595	.605
е	1.27 TYP		.050	TYP
Ĺ	6.30	6.40	.248	.252

NOTES:

- 1. The U.S. government preferred system of measurement is the metric SI. This item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
- 2. Pin 1 is indicated by the ESD triangle marked on top of the package.

FIGURE 1. Case outline.

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Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	DATA LOAD	19	AGND	37	BIT 9
2	VL _{I/O}	20	N/C	38	BIT 10
3	AGND	21	-SIN	39	BIT 11
4	V _{CC} or +5 VA	22	+SIN	40	BIT 12
5	VCOIN	23	AGND	41	BIT 13
6	INTIN2	24	-cos	42	BIT 14
7	N/C	25	+COS	43	BIT 15
8	INTIN1	26	DGND	44	BIT 16 (LSB)
9	INT1	27	V _{DD} or +5 VD	45	ENABLE
10	INT2	28	BIT 1 (MSB)	46	N/C
11	+REF	29	BIT 2	47	ĪNH
12	-REF	30	BIT 3	48	SC2
13	AC2	31	BIT 4	49	SC1
14	AC1	32	BIT 5	50	BUSY
15	BPF2	33	N/C	51	CW/CCW
16	BPF1	34	BIT 6	52	RIPPLE
17	DEMOD1	35	BIT 7		
18	DEMOD2	36	BIT 8		

FIGURE 2. <u>Terminal connections</u>.

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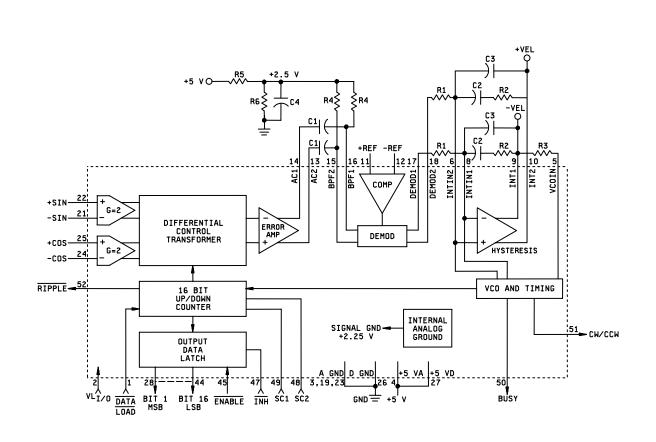


FIGURE 3. Block diagram.

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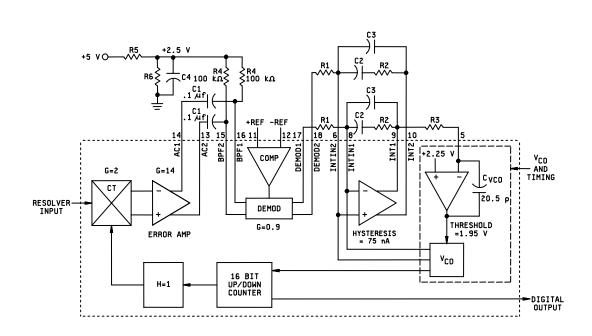


FIGURE 4. Functional block diagram.

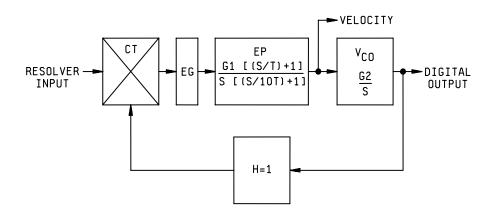


FIGURE 5. Transfer function diagram.

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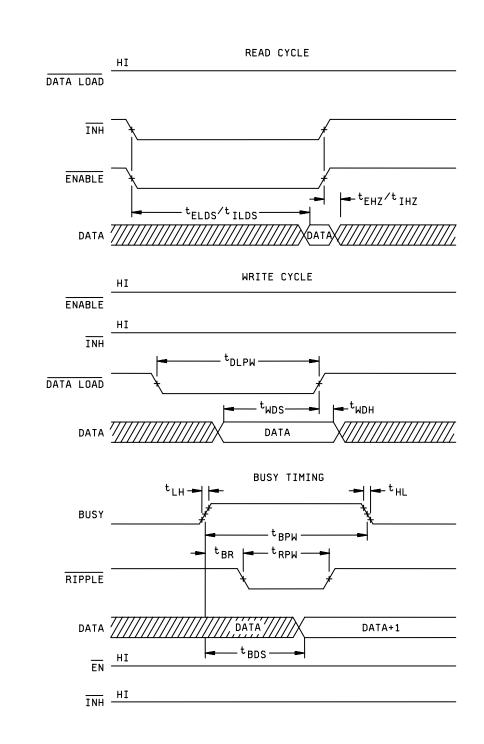


FIGURE 6. Timing diagram(s).

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TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	
Final electrical parameters	1*, 2, 3, 9, 10, 11
Group A test requirements	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters	1, 2, 3, 9, 10, 11
End-point electrical parameters for Radiation Hardness Assurance (RHA) devices	Not applicable

^{*} PDA applies to subgroup 1.

- 4.2 <u>Screening</u>. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:
 - a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.
 - b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.
- 4.3 <u>Conformance and periodic inspections</u>. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.
 - 4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:
 - a. Tests shall be as specified in table II herein.
 - b. Subgroups 4, 5, 6, 7, 8A, and 8B shall be omitted.
 - 4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

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- 4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:
 - a. End-point electrical parameters shall be as specified in table II herein.
 - b. Steady-state life test, method 1005 of MIL-STD-883.
 - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - (2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.
 - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
- 4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.
- 4.3.5 Radiation Hardness Assurance (RHA) inspection. RHA inspection is not currently applicable to this drawing.
- 5. PACKAGING
- 5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.
- 6. NOTES
- 6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.
- 6.2 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.
- 6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated as specified in MIL-PRF-38534.
- 6.4 <u>Record of users</u>. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.
- 6.5 <u>Comments</u>. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-1081.
- 6.6 <u>Sources of supply</u>. Sources of supply are listed in MIL-HDBK-103 and QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.
 - 6.7 Pin functions. Microcircuits conforming to this drawing shall have the pin functions as specified in table III herein.

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Table III. Pin functions.

SIGNAL	DIRECTION	PIN	SIGNAL DESCRIPTION
+SIN	INPUT	22	Analog Sine input from Synchro or Resolver. 1.3 V rms nominal
-SIN		21	
+COS	INPUT	25	Analog Cosine input from Synchro or Resolver. 1.3 V rms nominal
-COS		24	
+REF	INPUT	11	Analog Reference input
-REF		12	
BIT 1 (MSB)	BIDIR	28	Digital angle data. Parallel format. Natural binary positive logic.
BIT 2		29	Bit 1, most significant bit = 180° , Bit $2 = 90^{\circ}$, Bit $3 = 45^{\circ}$ and so on.
BIT 3		30	
BIT 4		31	In the 10 bit mode, Bit 10 is the LSB. Bits 11-16 are 0s.
BIT 5		32	In the 12 bit mode, Bit 12 is the LSB. Bits 13-16 are 0s.
BIT 6		34	In the 14 bit mode, Bit 14 is the LSB. Bits 15-16 are 0s.
BIT 7		35	In the 16 bit mode, Bit 16 is the LSB.
BIT 8		36	
BIT 9		37	
BIT 10		38	
BIT 11		39	
BIT 12		40	
BIT 13		41	
BIT 14 BIT 15		42	
		43 44	
BIT 16 (LSB) SC1	INPUT	49	Digital input. Sets the resolution.
SC2	INFOI	48	SC1 SC2 Resolution
302		40	0 0 10 bit
			0 1 12 bit
			1 0 14 bit
			1 1 16 bit
ENABLE	INPUT	45	Logic 0 enables digital angle output. Otherwise it is high impedance.
ĪNH	INPUT	47	Logic 0 freezes the digital angle output so that it can be safely read.
DATA LOAD	INPUT	1	Logic 0 enables the digital angle lines to be inputs to preset the angle. Logic 1 is for normal digital angle output.
BUSY	OUTPUT	50	A logic 1 pulse when the digital angle changes by 1 LSB.
CW/CCW	OUTPUT	51	For turns counting. Logic 1 = counting up (CW), logic 0 = counting down (CCW).
RIPPLE	OUTPUT	52	Ripple clock for turns counting. A logic 0 pulse = a 0° transition in either direction.

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Table III. Pin functions - Continued.

SIGNAL	DIRECTION	PIN	SIGNAL DESCRIPTION
AC1	OUTPUT	14	Differential AC error output
AC2		13	
BPF1	INPUT	16	Differential AC error input to demodulator
BPF2		15	
DEMOD1	OUTPUT	17	Differential DC error output
DEMOD2		18	
INTIN1	INPUT	8	Differential DC input to differential velocity integrator
INTIN2		6	
INT1	OUTPUT	9	Differential velocity output
INT 2		10	
VCOIN	INPUT	5	Input to Voltage Controlled Oscillator
V _{CC} or +5 VA	POWER	4	Analog Power In
V _{DD} or +5 VD		27	Digital Power In
A GND	POWER	3,19,23	Analog Power ground
D GND		26	Digital Power ground
VLi/o	POWER	2	Digital input/output DC power supply. Sets logic 1 level. +3V to +5V

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6.8 <u>Die anomalies</u>. There are two anomalies known for this device. The first anomaly is the instability at 360° and 180° input angles. This problem only occurs in the 16-bit mode when rotating in the clockwise direction and has been observed on 100 percent of the parts at 25°C. It occurs 100 percent of the time at 360° and approximately 76 percent at 180°. At 360° the problem occurs when the counter passes from FFFF to 0000 then reverse rotation counter clockwise back to FFFF. At 180° the problem occurs when the counter passes from EFFF to 8000 then reverse rotation counter clockwise back to EFFF. Two different failure modes have been observed for this anomaly and are as follows:

- 1). The output latch locks to a value with the most significant bit (MSB) inverted giving indication that the part is 180° out phase, the part exhibits zero error. This condition remains indefinitely until the resolver rotates in either direction by one count. At which time, the part responds to the 180° error which takes less than 150 milli-seconds to correct.
- 2). The part sees an immediate error of 180° and begins to correct this error which takes less than 150 milli-seconds.

In some cases it has been observed that the MSB is fine but the next bit gets inverted which provides a 90° error. In this case the time required for the part to correct itself is less than 75 milli-seconds.

The recommended actions to avoid this problem are as follows:

- 1). Use the 10, 12, or 14-bit mode.
- 2). Insure hysteresis of at least one bit to prevent this anomaly when rotating very slowly.
- 3). Avoid reversing direction at 360° and 180° when rotating in the clockwise direction.
- 4). If the resolver stops within two counts of 360° or 180° wait 150 milli-seconds after motion resumes before reading the parts output.

The second anomaly is correcting the Integral Nonlinearity Error . The following information is provided to address the constant Integral Nonlinearity (INL) that exists at each angle of the part. The error is repeatable from part to part and table IV of offsets is included herein that must be added to the output of the part to get the correct angle. Figure 7 shows the error in minutes that exist at 2° increments for the full 360°. The INL error from 0° to 180° is basically the same error between 180° to 360°. Table IV has the angle correction factor (in minutes) that must be added to zero out the INL error.

A simple calculation can be performed to derive a correction factor for angles that fall between the angles listed in table IV herein.

AL = Larger Angle AS = Smaller Angle

CL = Correction factor associated with Larger Angle
CS = Correction factor associated with Smaller Angle

NA = New Angle

NCF = New Correction Factor

Formula: NCF = CS + (((NA - AS) / (AL - AS)) * (CL - CS))

Example:

Require the correction factor at 15°

NCF = 23.4009 + (((15 - 14) / (16 - 14)) * (24.0326 - 23.4009))NCF = 23.4009 + (((1) / (2)) * .6137NCF = 23.4009 + (.5 * .6137)NCF = 23.4009 + .31585NCF = 23.71675 minutes

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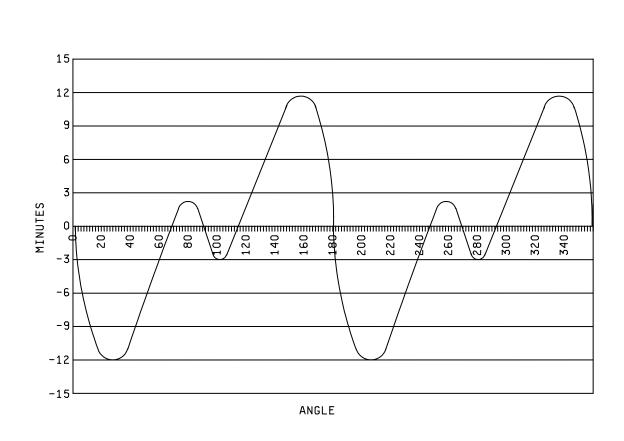


FIGURE 7. Anomaly 2, Angle Error Chart.

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Table IV. Anomaly 2, Correction Factor (minutes).

Angle	Correction Factor	Angle	Correction Factor	Angle	Correction Factor	Angle	Correction Factor
0	0.125244141	90	0.415283203	180	0.145019531	270	0.474609375
2	1.911621094	92	1.153564453	182	1.997314453	272	1.206298828
4	4.073730469	94	1.977539062	184	3.981445312	274	1.970947266
6	5.715087891	96	2.537841797	186	5.754638672	276	2.577392578
8	6.868652344	98	2.814697266	188	6.822509766	278	2.649902344
10	8.411132812	100	3.071777344	190	8.411132813	280	3.150878906
12	9.241699219	102	2.735595703	192	9.221923828	282	2.794921875
14	10.17114258	104	2.656494141	194	10.19750977	284	2.682861328
16	11.11376953	106	2.478515625	196	11.09399414	286	2.564208984
18	11.54882812	108	1.885253906	198	11.44995117	288	1.858886719
20	11.94433594	110	1.285400391	200	11.97729492	290	1.562255859
22	11.99707031	112	0.837158203	202	12.01025391	292	0.626220703
24	11.91137695	114	-0.243896484	204	11.88500977	294	-0.171386719
26	12.26733398	116	-0.626220703	206	12.19482422	296	-0.652587891
28	11.85205078	118	-1.621582031	208	12.10913086	298	-1.496337891
30	11.77954102	120	-2.168701172	210	11.82568359	300	-2.083007812
32	11.97070312	122	-2.814697266	212	11.92456055	302	-2.649902344
34	11.64770508	124	-3.460693359	214	11.64111328	304	-3.618896484
36	11.26538086	126	-4.548339844	216	11.22583008	306	-4.403320313
38	10.90942383	128	-4.871337891	218	10.89624023	308	-4.95703125
40	10.16455078	130	-5.945800781	220	10.13818359	310	-5.879882812
42	9.683349609	132	-6.842285156	222	9.650390625	312	-6.723632813
44	9.030761719	134	-7.48828125	224	8.984619141	314	-7.461914063
46	8.002441406	136	-8.582519531	226	7.969482422	316	-8.450683594
48	7.237792969	138	-9.043945313	228	7.218017578	318	-8.918701172
50	6.545654297	140	-9.887695313	230	6.492919922	320	-9.755859375
52	5.6953125	142	-10.31616211	232	5.682128906	322	-10.29638672
54	5.174560547	144	-10.73144531	234	5.174560547	324	-10.81054687
56	4.198974609	146	-11.15332031	236	4.185791016	326	-11.29174805
58	3.487060547	148	-11.43017578	238	3.520019531	328	-11.3972168
60	2.939941406	150	-11.32470703	240	2.887207031	330	-11.44995117
62	2.241210938	152	-11.64770508	242	2.181884766	332	-11.57519531

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Table IV. Anomaly 2, Correction Factor (minutes) -Continued.

Angle	Correction Factor	Angle	Correction Factor	Angle	Correction Factor	Angle	Correction Factor
64	1.614990234	154	-11.70043945	244	1.588623047	334	-11.65429688
66	1.087646484	156	-11.71362305	246	1.114013672	336	-11.62792969
68	0.131835938	158	-11.5949707	248	0.171386719	338	-11.62792969
70	-0.547119141	160	-11.58837891	250	-0.573486328	340	-11.56201172
72	-1.0546875	162	-11.1862793	252	-1.074462891	342	-11.12036133
74	-1.549072266	164	-10.79077148	254	-1.502929687	344	-10.81713867
76	-1.641357422	166	-9.861328125	256	-1.628173828	346	-9.834960938
78	-1.977539063	168	-8.971435547	258	-1.984130859	348	-8.978027344
80	-1.944580078	170	-7.929931641	260	-1.957763672	350	-7.883789063
82	-1.766601563	172	-6.512695313	262	-1.713867188	352	-6.473144531
84	-1.753417969	174	-5.510742187	264	-1.694091797	354	-5.444824219
86	-1.0546875	176	-3.697998047	266	-1.034912109	356	-3.684814453
88	-0.250488281	178	-1.680908203	268	-0.283447266	358	-1.654541016

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 04-10-01

Approved sources of supply for SMD 5962-04235 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534.

Standard	Vendor	Vendor
microcircuit drawing	CAGE	similar
PIN <u>1</u> /	number	PIN <u>2</u> /
5962-0423501KXA	88379	ACT5028-201-2S
5962-0423501KXC	88379	ACT5028-201-1S

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.
- 2/ <u>Caution</u>. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE __number_

88379 Aeroflex Circuit Technology Corporation 35 South Service Road

35 South Service Roa Plainview, NY 11803

Vendor name and address

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.